**Listing of Claims**

Claim 1 (currently amended). A tracing method, comprising:

~~obtaining at least one indication of a tracing condition, wherein a tracing condition defines a tracing control based upon a characteristic of an operating state of a processor;~~

detecting ~~a change in said characteristic of said~~ an operating state of ~~said~~ a processor, said processor having a plurality of operating states that include a plurality of processor modes; and

effecting a predefined tracing control based on ~~said detected change in said characteristic of said~~ a current operating state of said processor and upon a control input for said current operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state.

Claim 2 (currently amended). The method of claim 1, wherein ~~an indication is obtained via~~ an indication of said control input for said current operating state is obtained via an input control signal.

Claim 3 (currently amended). The method of claim 1, wherein ~~an indication is obtained~~ an indication of said control input for said current operating state is obtained via a software-settable trace control register.

Claim 4 (canceled)

Claim 5 (currently amended). The method of claim [[4]] 1, wherein said processor ~~mode is~~ modes comprise at least one of a kernel mode, a supervisor mode, a user mode, and a debug mode.

Claim 6 (currently amended). The method of claim 5, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on ~~the MIPS32 and MIPS 64~~ a MIPS32™ or MIPS64™ architecture specification ~~specifications~~.

Claim 7 (currently amended). The method of claim 1, wherein said ~~characteristic is~~ at least one operating state includes an identity of a process being run on said processor and said predefined trace control is based on a current processor mode and said identity of a process.

Claim 8 (original). The method of claim 1, wherein said effecting comprises initiating tracing.

Claim 9 (original). The method of claim 1, wherein said effecting comprises inhibiting tracing.

Claim 10 (currently amended). The method of claim 1, wherein said operating states include an identity of a process running on said processor and tracing is triggered based on G, ASID, U, K, S, DM, and X controls, wherein said G if asserted, implies that

all processes are to be traced, whereas if G is not asserted, trace data is processed for a current ASID value, ASID is an application space identity, U, if asserted, enables tracing in user mode, K, if asserted enables tracing in kernel mode, S, if asserted, enables tracing in supervisor mode, DM, if asserted, enable tracing in a debug mode, and X, if asserted, enables tracing for exception and error level conditions, said controls enabling tracing when:

((G is asserted OR (ASID equals a current process application space identity value)) AND

((U is asserted AND said processor is in user mode) ~~AND~~ OR

(K is asserted AND said processor is in kernel mode) ~~AND~~ OR

(S is asserted AND said processor is in supervisor mode) ~~AND~~ OR

(DM is asserted AND said processor is in debug mode) ~~AND~~ OR

(X is asserted AND (an exception level bit is asserted OR an error level bit is asserted)).

Claim 11 (currently amended). A tracing system, comprising:

a processor core for executing instructions; and

trace generation logic that detects ~~a change in a characteristic of~~ an operating state of said processor core said processor core having a plurality of operating states that include a plurality of processor modes, said trace generation logic effecting a predefined tracing control based on ~~said detected change in said characteristic of said~~ a current operating state of said processor and upon a control input for said operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is

automatically adjusted when said processor transitions from one operating state to another operating state.

Claim 12 (currently amended). The tracing system of claim 11, wherein said ~~predefined tracing control~~ control input is identified via an input control signal.

Claim 13 (currently amended). The tracing system of claim 11, wherein said ~~predefined tracing control~~ control input is identified via a software-settable control register.

Claim 14 (canceled).

Claim 15 (currently amended). The tracing system of claim [[14]] 11, wherein said processor modes include at least ~~mode is~~ one of a kernel mode, a supervisor mode, a user mode, and a debug mode.

Claim 16 (currently amended). The tracing system of claim 15, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on ~~the MIPS32 and MIPS 64~~ a MIPS32™ or MIPS64™ architecture specification ~~specifications~~.

Claim 17 (currently amended). The tracing system of claim 11, wherein said ~~characteristic is~~ operating state includes an identity of a process being run on said

processor and said predefined trace control is based on a current processor mode and said identity of a process.

Claim 18 (currently amended). The tracing system of claim 11, wherein said trace generation logic initiates tracing for said predefined tracing control ~~based on said detected change in said characteristic of said operating state of said processor~~.

Claim 19 (currently amended). The tracing system of claim 11, wherein said trace generation logic inhibits tracing for said predefined tracing control ~~based on said detected change in said characteristic of said operating state of said processor~~.

Claim 20 (currently amended). The tracing system of claim 11, wherein said trace generation logic triggers tracing based on G, ASID, U, K, S, DM, and X controls, wherein said G if asserted, implies that all processes are to be traced, whereas if G is not asserted, trace data is processed for a current ASID value, ASID is an application space identity, U, if asserted, enables tracing in user mode, K, if asserted enables tracing in kernel mode, S, if asserted enables tracing in supervisor mode, DM, if asserted, enable tracing in a debug mode, and X, if asserted, enables tracing for exception and error level conditions, said controls enabling tracing when:

((G is asserted OR (ASID equals a current process application space identity value)) AND

((U is asserted AND said processor is in user mode) ~~AND~~ OR

(K is asserted AND said processor is in kernel mode) ~~AND~~ OR

(S is asserted AND said processor is in supervisor mode) ~~AND~~ OR

(DM is asserted AND said processor is in debug mode) ~~AND~~ OR

(X is asserted AND (an exception level bit is asserted OR an error level bit is asserted)).

Claim 21 (currently amended). A computer program product comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a trace generation logic that detects ~~a change in a characteristic of~~ an operating state of said processor core said processor core having a plurality of operating states that include a plurality of processor modes, said trace generation logic effecting a predefined tracing control based on ~~said detected change in said characteristic of said~~ a current operating state of said processor and upon a control input for said operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state; and

a computer-usable medium configured to store the computer-readable program codes.

Claim 22 (currently amended). A method for enabling a computer to generate a tracing system, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a trace generation logic that detects ~~a change in a characteristic of~~ an operating state of said processor core said processor core having a plurality of operating states that include a plurality of processor modes, said trace generation logic effecting a predefined tracing control based on ~~said detected change in said characteristic of said~~ a current operating state of said processor and upon a control input for said operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state.

Claim 23 (original). The method of claim 22, wherein computer-readable program code is transmitted to said computer over the Internet.

Claim 24 (currently amended). A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a trace generation logic that detects ~~a change in a characteristic of~~ an operating state of said processor core said processor core having a plurality of operating states that include a plurality of processor modes, said trace generation logic effecting a predefined tracing

control based on ~~said detected change in said characteristic of said~~ a current operating state of said processor and upon a control input for said operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state.